

CLAIMS

What is claimed is:

- 1 1. A radio frequency (RF) power amplifier, comprising:
 - 2 a first, a second, a third, a fourth, a fifth, and a sixth transistor, each having a
 - 3 drain, a source, and a gate; and
 - 4 a first, a second, a third, and a fourth resistor;
 - 5 the drain of the first transistor coupled to the sources of the second and third
 - 6 transistors and, the drain of the second transistor coupled to the gate of the second transistor
 - 7 via the first resistor, the gate of the second transistor coupled to the gate of the fifth transistor
 - 8 via the second resistor,
 - 9 the drain of the fourth transistor coupled to the sources of the fifth and sixth
 - 10 transistors and, the drain of the fifth transistor coupled to the gate of the fifth transistor via
 - 11 the third resistor, the gate of the fifth transistor coupled to the gate of the third transistor via
 - 12 the fourth resistor, the fourth resistor coupled to the gate of the third transistor and the second
 - 13 resistor coupled to the gate of the sixth transistor.
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- 1 2. A system, comprising:
 - 2 a radio frequency (RF) power amplifier; and
 - 3 a digital conduction angle circuitry merged with the RF power amplifier.
- 1 3. The system of claim 2, wherein the digital conduction angle circuitry comprises
- 2 multiple inverter branches of p-type metal oxide semiconductor (PMOS) and n-type MOS
- 3 (NMOS) switches coupled to the RF power amplifier.
- 1 4. The system of claim 2, wherein the PMOS and NMOS inverter branches include a
- 2 logical “1” state or a logical “0” state.
- 1 5. The system of claim 2, wherein the RF power amplifier includes a self-biased cascode

2 stage.

1 6. The system of claim 5, wherein the RF power amplifier includes a driver stage.

1 7. The system of claim 2, further comprising a digital control function coupled to the RF
2 power amplifier.

1 8. The system of claim 2, further comprising a digital control function coupled to the
2 digital conduction angle tuning circuitry.

1 9. A radio frequency (RF) power amplifier, comprising:
2 a driver stage; and

3 a self-biased cascode stage coupled to the driver stage, the self-biased cascode
4 stage including a first transistor, a second transistor, a third transistor, a fourth transistor, a
5 fifth transistor, and a sixth transistor, each having a drain, a source, and a gate, the drain of
6 the first transistor coupled to the sources of the second and third transistors, the gate of the
7 first transistor coupled to the driver stage, the drain of the second transistor coupled to the
8 gate of the second transistor via the first resistor, and the gate of the second transistor coupled
9 to the gate of the fifth transistor via the second resistor.

1 10. The RF power amplifier of claim 9, further comprising a second driver stage coupled
2 to the self-biased cascode stage.

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1 11. The RF power amplifier of claim 9, wherein the driver stage is an inverter-type class
2 B amplifier.

1 12. A method of operating a radio frequency (RF) power amplifier, comprising:
2 digitally programming a radio frequency (RF) power amplifier conduction
3 angle;

4 applying an analog information signal to the RF power amplifier; and
5 operating the RF power amplifier at the conduction angle specified by the
6 digital programming.

1 13. The method of claim 12, wherein digitally programming a radio frequency (RF)
2 power amplifier conduction angle comprises coupling a combination of PMOS and NMOS
3 switches to a driver stage of the power amplifier.